REMARKS/ARGUMENT

Claim objections:

Claims 26 & 27 have been amended to depend from Claim 24. As such, the objection is overcome.

Double Patent rejection:

1) Claims 17, 28-35 and 37-38 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8-15 of copending Application No. 11/388,558. Applicants traverse the rejection as follows:

In rejecting Claims 17, 28-35 and 37-38 the Examiner has not appropriately compared Claims 17, 28-35 and 37-38 of the present application with Claims 8-15 of copending Application No. 11/388,558. The Examiner makes the following determination:

> Although the conflicting claims are not identical, they are not patentably distinct from each other because both inventions recites the cascade of IIR filters comprising: a first capacitor; a first rotary capacitor; a second rotary capacitor; a buffer capacitor; and a negative feedback loop (Office Action page 2, line 29 – page 3, line 8).

Applicants respectfully submit that the Examiner has not established a prima facie case of obviousness-type double patenting for Claims 17, 28-35 and 37-38. In order to establish a prima facie case of obviousness-type double patenting, **the Examiner must establish that the claims of the present application are obvious over the CLAIMS of the cited application** (in this case Application No. 11/388,558). Applicants direct the Examiner's attention to MPEP § 804(B)(1):

In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is – **does any claim in the application define an invention that is merely an obvious variation of an invention claimed in the patent**? If the answer is yes, then an "obvious-type" nonstatutory double patent rejection may be appropriate.

(A) Determine the scope and content of a patent claim and the prior art relative to a claim in the application at issue;

(B) Determine the **differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue**;

(C) **Determine the level of ordinary skill in the pertinent art**; and

(D) **Evaluate any objective indicia of nonobviousness**.

The conclusion of obvious-type double patenting is made in light of these factual determinations.

Any obvious-type double patent rejection should make clear:

(A) The **differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application**; and

(B) The **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**.

When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, **the disclosure of the patent may not be used as prior art**. This does not mean that one is precluded from all use of the patent disclosure.

Applicants respectfully submit that the Examiner has not: (B) Determined the **differences between the scope and content of the claims of the copending applications and the prior art as determined in (A) and the claims in the application at issue**; (C) **Determined the level of ordinary skill in the pertinent art**; and (D) **Evaluate any objective indicia of nonobviousness**. Moreover, Applicants respectfully submit that the Examiner has not completely identified the **differences between the inventions defined by the conflicting claims – each claim in the co-pending applications compared to the claims in the present application**.

as required by (A) above and has not provided **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**, as required in (B) above. For these reasons alone, the double-patenting rejection is improper and must be withdrawn. Moreover, even had the double-patenting rejection been set forth in the required manner, the rejection is improper for the following reasons:

As an example, Claim 17 of the present application is reproduced below:

17. A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first **set of** rotating capacitors, **wherein at least one of the rotating capacitors is connected to the history capacitor**;

a buffer capacitor **connected to at least one of the rotating capacitors other than the at least one of the rotating capacitors connected to the history capacitor**; and

a second **set of** rotating capacitors, wherein **at least one of the second set of rotating capacitors is connected to the buffer capacitor**.

Whereas the combination of Claims 1 & 8 of copending Application No. 11/388,558 is reproduced below:

8. A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises a history capacitor **that is charged together with** a first rotating capacitor **in a first capacitor bank for a predetermined time period while a charge in a second capacitor bank is charge shared with a buffer capacitor** and a

second rotating capacitor, **and wherein during a subsequent time period, the first capacitor bank holding its charge is charge shared with the buffer capacitor while the second capacitor bank which was charge shared in a previous time period now collects new samples together with the history capacitor.**

The above language in bold in each claim is not found in the other claim. As such, Examiner has not compared all of the words of Claim 17 of the present application with Claim 8 of copending Application No. 11/388,558, as required by law.

Similarly, Examiner has not appropriately compared Claims 28-35, 37 and 38, of the present application with claims 9-15 of copending Application No. 11/388,558, as required by law. Accordingly, Examiner's double patent rejection is improper and must be withdrawn.

2) Claims 2-3 and 6-16, 19 and 39 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3, 6, 7 , 21, 22 and 23 of copending Application No. 11/388,558 in view of Yasuda. Applicants traverse this rejection as set forth below.

In rejecting Claims 2-3 and 6-16, 19 and 39 the Examiner has not appropriately compared Claims 2-3 and 6-16, 19 and 39 of the present application with Claims 1-3, 6, 7, 21, 22 and 23 of copending Application No. 11/388,558. The Examiner makes the following determination:

> The application ('558) recites a cascade of IIR filters circuit but does not recite that the IIR filters are comprised solely capacitors and switches. Nevertheless, Yasuda suggest in Figure 9 the IIR filter which is comprised solely switches (SW11-SW1n) and capacitors (C11-C1n), see lines 65-67, column 4 for being implemented on an IC, lines 1-6, column 5. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporated the suggestion of Yasuda into the application ('558) for the purpose of being implemented on an IC. Regarding claims 19 and 39,

> selecting the optimum number of two rotary capacitors for the purpose of accommodating with requirement of a predetermined system is considered to be a matter of design for an engineer that would have been obvious at the time of the invention (Office Action, page 3, line 14 – page 4, line 3).

Applicants respectfully submit that the Examiner has not established a prima facie case of obviousness-type double patenting for Claims 2-3 and 6-16, 19 and 39. In order to establish a prima facie case of obviousness-type double patenting, **the Examiner must establish that the claims of the present application are obvious over the CLAIMS of the cited application** (in this case Application No. 11/388,558) in view of Yasuda (US 6,181,740). Applicants direct the Examiner's attention to MPEP § 804(B)(1):

> In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is – **does any claim in the application define an invention that is merely an obvious variation of an invention claimed in the patent**? If the answer is yes, then an "obvious-type" nonstatutory double patent rejection may be appropriate.
>
> (A) Determine the scope and content of a patent claim and the prior art relative to a claim in the application at issue;
>
> (B) Determine the **differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue**;
>
> (C) **Determine the level of ordinary skill in the pertinent art**; and
>
> (D) **Evaluate any objective indicia of nonobviousness**.
>
> The conclusion of obvious-type double patenting is made in light of these factual determinations.
>
> Any obvious-type double patent rejection should make clear:
>
> (A) The **differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application**; and
>
> (B) The **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**.
>
> When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a

patent, **the disclosure of the patent may not be used as prior art**. This does not mean that one is precluded from all use of the patent disclosure.

Applicants respectfully submit that the Examiner has not: (B) Determined the **differences between the scope and content of the claims of the copending applications and the prior art as determined in (A) and the claims in the application at issue**; (C) **Determined the level of ordinary skill in the pertinent art**; and (D) **Evaluate any objective indicia of nonobviousness**. Moreover, Applicants respectfully submit that the Examiner has not completely identified the **differences between the inventions defined by the conflicting claims – each claim in the co-pending applications compared to the claims in the present application**, as required by (A) above and has not provided **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**, as required in (B) above. For these reasons alone, the double-patenting rejection is improper and must be withdrawn.

Independent Claim 16 of the present invention requires and positively recites a discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**.

Independent Claim 1 of copending Application No. 11/388,558 requires and positively recites, a discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal.

Examiner admits that copending Application No. 11/388,558 fails to teach or suggest, "**wherein the single pole IIR filters are comprised solely of switches and capacitors**". Examiner relies upon Yasuda as providing such teaching that one having ordinary skill in the

would look to for combining with Claims 1 of copending Application No. 11/388,558. Applicants respectfully traverse this determination as set forth below.

Yasuda proposes a sampling system that embeds an analog decimation filter composed of an FIR filter (col. 2, lines 33-48; col. 3, lines 20-30) with the purpose of providing anti-alis filtering to noise folding inherent in sub-sampling receivers. While true that a filter can be realized using capacitors and switches only, Yasuda addresses finite-impulse response filter design that is obtained by combining weighted sum of input samples in a window of n samples (sampled on C11 to C1n) to obtain anti-aliasing filtering for noise folding due to decimation. This is clearly described in the Yasuda's Abstract and in the body of the Specification. Each time C11 to C1n sample the input, the sample-and-hold operation discards (over-writes) the previous input and this arrangement cannot provide an infinite-impulse response that relies on a sampler that maintains the history of sampled charge for infinite previous samples as is suggested in the present application.

Yasuda similarly fails to provide any means for integration of previous samples on the sampling capacitors, since the sampling capacitor is driven by a LNA through a bandpass filter, that presents an input voltage that is sampled on to the sampling capacitor. Even if n samples can be sampled and combined together when presented to the summing amplifier, however, the response is FIR followed immediately by decimation by n, since 1 output is produced for every n inputs. The weighting of individual samples can be done as shown in FIG. 8, however, the system can only provide FIR response, since there is no means for accumulating samples in an infinite window. Therefore, Applicants respectfully Examiner's assessment that Yasuda suggests an IIR filter, since an IIR filter must have a memory element that maintains some information of all the previous samples, hence, providing an infinite impulse response.

In contrast to Yasuda technique for producing only 1 output for every n inputs, the present invention can produce 1 output for every 1 input and n consecutive outputs for n

consecutive inputs (see equation 2). It is not suggested by Yasuda et. al. on how to obtain one output for every 1 input, while providing a filtering response.

Page 5, paragraph 1, discloses that that reference US 2003/0035499 A1 entitled Direct Radio Frequency (RF) Sampling With Recursive Filtering Method that is included in its entirety. This application describes the fundamental operation of sampling by means of converting the RF voltage to an RF current through the LNTA (Low noise trans-conductance amplifier) and integrating the current on to the sampling capacitor. The LNTA is described as a two stage RF amplifier in which the first stage is a voltage amplifier (LNA) followed by a V-I converter (through using the trans-conductance element to convert voltage output of LNA to current that charges the sampling capacitor CH) that constitutes the second stage. The sampling operation at the input of the PIIR is described to be of integration of RF current – not the sample-and-hold proposed by Yasuda or the other cited references of prior art in the office action. This summary of the operation is described on Page 5 in lines 10-25.

Yasuda also does not present a history and a rotating capacitor to obtain an IIR filter response, and provides no teaching or suggestion why one having ordinary skill in the art at the time of the invention would want to modify the Yasuda apparatus, such as the one described by equations 1, 2, 3, 6 and following descriptions on Page 8, lines 23 onwards in the present application which describe the system in which the rotating capacitor is never discharged. As such, one having ordinary skill in the art at the time of the invention would not have been motivated to combine Yasuda with the teaching Claim 1 in order to arrive at Claim 16 of the present application. As such, the double patenting rejection of Claim 16 is improper and must be withdrawn.

Claims 2-3 and 6-15 depend directly, or indirectly, from Claim 16. As such the double patenting rejection of Claims 2-3 and 6-15 must also be withdrawn.

Regarding Claims 19 and 39, Applicants respectfully traverse Examiner's determination. To maintain a constant flow of charge from CH towards CB1 and CB2, as one rotating capacitor samples the input together with CH, the other presents the previous sample to CB1. Similarly, as the second rotating capacitor samples the input from CB1, the second rotating capacitor provides the input to CB2. This maintains a constant rate of flow of samples, such that each input sample to CH can produce a sample at CB2, without any decimation. Hence, filtering is achieved without decimating samples.

US 2003/0035499 describes decimation on to CH only. However, no further decimation occurs in the proposed PIIR stages, independent of the number of cascaded stages. Accordingly, the double patenting rejection of Claims 19 and 39 is improper and must be withdrawn.

35 U.S.C. 102(b) rejections:

1) Claims 2, 4, 6, 7, 16 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasuda (US 6,181,740). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 2, 4, 6, 7, 16 and 24 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 4 requires and positively recites a high order filter comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**".

Independent Claim 16 requires and positively recites, a discrete time analog filter comprising a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **single pole IIR filters** are comprised solely of switches and capacitors.

Independent Claim 24 requires and positively recites, a receiver front-end comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**, wherein the cascade of **single pole IIR filters**, the means for direct sampling, and the at least one amplifier stage together implement a high order filter".

In contrast, Yasuda does not disclose or even remotely suggest an IIR filter in Figures 3 or 9 which only show sample-and-hold circuits sampling input voltage (see col. 10, lines 50 onwards), providing an input to a sigma-delta A/D converter that accepts the input from the plurality of these sample and hold circuits. No "history capacitor" is available in such configurations to provide IIR filtering function. Even if FIR filtering could be achieved in Yasuda by combining samples as they are sampled to the input of the A/D converter (see col. 11), sampling n consecutive samples on n distinct capacitors and combining a weighted average of these would not provide an IIR response! One window

of n samples does not affect the output produced by the next window of n samples. IIR filtering is neither anticipated by Yasuda, not implied or remotely suggested. No means are provided in Yasuda to achieve such a response. Accordingly, the 35 U.S.C. 102(b) rejection of Claims 4, 16 and 24 is improper and must be withdrawn.

Claims 2, 6 and 7 stand allowable as depending from allowable claims and by including further limitations not taught or suggested by Yasuda.

Claim 2 further defines the discrete time analog filter according to claim 16, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers. Claim 2 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 6 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers. Claim 6 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 7 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage. Claim 7 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

2) Claim 28 is rejected under 35 U.S.C. 102(b) as being anticipated by Arvidsson et al. (US 6,414,541). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claim 28 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states. "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 28 requires and positively recites, a receiver front-end comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **cascade of single pole IIR filters** comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

In contrast, Arvidsson does not propose cascading IIR filters. Arvidsson discloses only one stage of IIR filter as explained by the recursive equation in col. 1, line 32. In his disclosure, Arvidsson proposes a means for sampling an input on C1 together with a rotating capacitor. Arvidsson then disconnects the rotating capacitor from the input and shows a means for multiplying the sample on the rotating capacitor by a factor less than 1, thereby providing an increased resolution, that would otherwise be only obtainable by placing numerous equal-sized part capacitors as he explains in col. 1 in the BACKGROUND section.

C1-C6 do not provide a filter pole, as suggested by Examiner. On the contrary, C1-C6 provide a means for dividing the input sample to obtain a fractional-sample to help

realize a higher resolution that would otherwise be only available using a large bank of sampling capacitor.

As such, Arvidsson provides no teaching of cascading filter stages. Arvidsson similarly provides no teaching of maintaining a constant rate of information flow through cascaded filter stages. Applicants note that C2-C6 also show reset switches, while C1 has no reset switch. Hence, CB1 or CB2 are not implied, or suggested, since the "memory" of previous inputs must be maintained by a sampling capacitor that is never discharged in order to obtain an IIR response. For cascaded filtering stages, there must me more than one capacitor that is never reset such as the case with CB1 and CB2 in the present application. A constant rate of information flow must be maintained, and hence, at least two rotating capacitors are needed to transport charge from one stage to the next. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 28 is improper and must be withdrawn.

35 U.S.C. 103(a) rejections:

1) Claims 6-7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simon et al (GB 2230627) in view of Yasuda (US 6,181,740). Applicants respectfully traverse this rejection as follows:

Independent Claim 16, requires and positively recites a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**.

Simon discloses a recursive processor that is used as a first order section IIR filter. To obtain a "cascaded" second or third order section IIR filter, more processors coupled

together in cascaded form are required. Examiner admits that Simon does not teach or suggest that the filters comprise solely of switches and capacitors (Office Action, page 5, lines 22-23). Examiner, however, relies upon Yasuda as disclosing in Figure 9 the IIR filter which is comprised solely of switches (SW11-SWin) and capacitors (C11-C1n). Applicants traverse this rejection as set forth below.

As stated previously by Applicants, Yasuda does not disclose, suggest or imply creating an IIR filter. No means for creating an IIR filter response can be inferred from Yasuda's disclosure. Furthermore, Simon et. al in GB2230627 addresses a digital IIR filter that is a completely different topic. A digital IIR filter is constructed by abstraction of bits to represent values and have no notion of "loading" effects from one stage to another. A switched capacitor based PIIR stage cannot be inferred from a digital filter. Maintaining integrity of analog samples, splitting and re-combining charge from one PIIR stage to another to obtain an IIR response is not deducible from studying a digital IIR filter. Maintaining a constant rate of information flow in which each input to the cascaded PIIR filtering stages produces an output, without incurring decimation or noise folding is not deducible by studying a digital filter implementation. Furthermore, improving gain by not resetting the rotating capacitors is also not deducible by studying digital filter implementations that are completely divorced from analog considerations and implementation aspects.

As such, any combination of Simon and Yasuda fails to teach or suggest, "a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**", as required by Claim 16. As such, the 35 U.S.C. 103(a) rejection of Claim 16 is improper and must be withdrawn.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re

Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Intereonnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). It is clear from the above analysis that the Examiner has not met his burden of **showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.** As such, a prima facie case of the obviousness of Claim 16 over a combination of Simon and Yasuda has not been shown.

Claims 6 and 7 stand allowable as depending from allowable claims and by including further limitations not taught or suggested by any combination of Simon and Yasuda.

Claim 6 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers. Claim 6 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 7 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage. Claim 7 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

2) Claims 6-7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 5,732,002) in view of Yasuda (US 6,181,740). Applicants respectfully traverse this rejection as follows:

Independent Claim 16, requires and positively recites a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**.

In contrast, Lee discloses present multi-rate IIR decimation and interpolation filters that are implemented in digital domain. Hence, Lee discloses constructing digital filters that process bits that abstract integers. Cascading digital filters is not straight-forward

from such teaching since there are no analog effects to be considered. A following stage does not "load" the previous stage and there is no notion of loss of charge or introduction of noise in the processed samples as long as enough bits are allocated to represent the digital values. In addition, Examiner admits that Lee does not disclose that the filters comprise solely of switches and capacitors (page 6, lines 14-15). Examiner, however, relies upon Yasuda for such teaching.

Yasuda, however, does not address an IIR filter construction as has been explained above. Cascading of IIR filter stages using switches and capacitors only is not addressed in either of these disclosures, neither suggested or hinted, nor inferable as means for achieving IIR filtering response are absent from Yasuda's disclosure.

As such, any combination of Lee and Yasuda fails to teach or suggest, "a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**", as required by Claim 16. As such, the 35 U.S.C. 103(a) rejection of Claim 16 is improper and must be withdrawn. Claims 6 and 7 stand allowable as depending from allowable claims and by including further limitations not taught or suggested by Yasuda.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). It is clear from the above analysis that the Examiner has not met his burden of **showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.** As such, a prima facie case of the obviousness of Claim 16 over a combination of Lee and Yasuda has not been shown.

Claim 6 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers. Claim 6 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 7 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage. Claim 7 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Applicants appreciate the Examiner indication that Claims 5, 18, 20, 25 and 40 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. However, for the reasons set forth above, Applicants believe Claims 5, 18, 20, 25 and 40 are allowable in their present form.

Accordingly, Claims 2-20, 24-35 and 37-40 stand allowable. Applicants respectfully request withdrawal of the rejections and allowance of the application as the earliest possible date.

Respectfully submitted,

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